

1 1. A packaged integrated circuit comprising:
2 a processor;
3 a volatile memory; and
4 a cross-point memory.

1 2. The circuit of claim 1 including a first die and
2 a second die, wherein said processor is on said first die
3 and said cross-point memory is on said second die.

1 3. The circuit of claim 2 wherein said first die
2 includes a processor and a bus that couples said processor
3 to the volatile memory and the cross-point memory.

1 4. The circuit of claim 1 also including a phase-
2 change memory.

1 5. The circuit of claim 1 including a package
2 containing stacked dice.

1 6. The circuit of claim 1 wherein said package is a
2 folded stacked package.

1 7. The circuit of claim 2 wherein said first die
2 includes a processor and a non-volatile memory.

1 8. The circuit of claim 1 including a non-volatile
2 memory.

 9. The circuit of claim 1 including a ball grid
array package.

1 10. A method comprising:
2 providing a processor and a cross-point memory on
3 separate dice; and
4 packaging said cross-point memory and said
5 processor in the same package.

1 11. The method of claim 10 including packaging a
2 volatile memory on a separate die in said package.

1 12. The method of claim 10 including packaging said
2 processor and said cross-point memory in a folded stacked
3 package.

1 13. The method of claim 10 including packaging a
2 phase-change memory in said package.

1 14. The method of claim 10 including providing a bus
2 on said die with said processor and coupling said processor
3 to said cross-point memory through said bus.

1 15. The method of claim 10 including stacking said
2 dice on top of one another.

1 16. The method of claim 10 including packaging a
2 volatile memory in the same package with said processor and
3 said cross-point memory.

1 17. The method of claim 10 including providing a ball
2 grid array on said package.

1 18. A packaged integrated circuit comprising:
2 a first die including a processor; and
3 a second die including a cross-point memory.

1 19. The circuit of claim 18 including a third die
2 with a volatile memory.

1 20. The circuit of claim 18 including a bus on said
2 first die coupling said processor to said cross-point
3 memory.

1 21. The circuit of claim 18 including a phase-change
2 memory.

1 22. The circuit of claim 18 including a plurality of
2 stacked dice.

1 23. The circuit of claim 18 including a folded
2 stacked package.

1 24. The circuit of claim 18 including a ball grid
2 array package.